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Interleaved Boost Converter under Alternating Phase Shift and Interleaving Control

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ABSTRACT

This paper investigates a PWM scheme for two-phase interleaved boost converter with avoltage multiplier for renewable energy systems by combining two methods such as Alternating Phase Shift (APS) control and traditional interleaving PWM control. The APS control is used to reduce the voltage stress on switches while the traditional interleaving control is used to keep better performance. The boundary condition for swapping between APS and traditional interleaving PWM control is derived. Based on simulation studies, a full power range control combining APS and thetraditional interleaving control are achieved.

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INTRODUCTION

With increasing concern about energy and environment, it is necessary to explore the renewable energy including wind power, solar, fuel cell, etc. The DC/DC converter generate a high frequency input current ripple, which will reduce the lifetime of the fuel cell stack High step-up ratio can be achieved by combining classical boost converter with switched inductors (Axelrod, B., 2008), coupled inductors (Qun, Z. and F.C. Lee, 2003), high frequency transformer (Changwoo, Y., 2011) or switched capacitor (SC) (Fardoun, A.A. and E.H. Ismail, 2010; Prudente, M., 2008; Gules, R., 2003). It obtains high step-up ratio with high efficiency, low voltage stress, and low EMI. Interleaving the DC/DC converter can reduce the input current ripple of the DC/DC converter. An interleaved boost converter with avoltage multiplier has been proposed in (Gules, R., 2003). Besides it has lower input current ripples and output voltage ripples in comparison to the conventional boost converter. An interleaved boost converter with avoltage multiplier was proposed in. Its voltage gain was increased up to (M +1) times (M is the number of the voltage multiplier) of the classical boost converter with the same duty-cycle D and lower voltage stress. Besides it has lower input current ripples and output voltage ripples in comparison to the conventional boost converter.

The interleaving boost converter with voltage multipliers is shown in Fig. 1. The converter is shown in Fig. One can achieve low voltage stress in the power devices, which increases the conversion efficiency which is only true in heavyload while the voltage stress of the power devices increases when it works in discontinuous mode (DCM).These authorsproposed a new method, named as AlternatingPhase Shift (APS), to overcome the problem when theconverter operatesat light load.

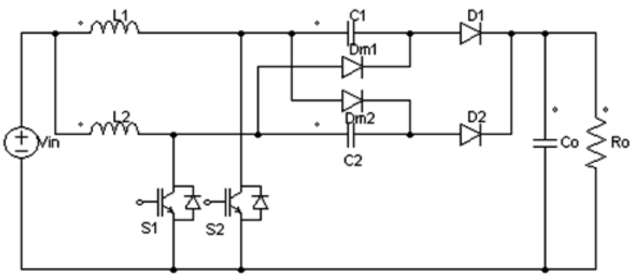

Fig. 1: Circuit diagram of two-phase interleaved boost converter.

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This paper investigates a PWM scheme fortwo-phase interleaved boost converter with avoltage multiplier for renewable energy System by combining APS and traditional interleaving PWM control. The APS control is used to reduce the voltage stress on switches in light load while the traditional interleaving poweris used to keep better performance in heavy load. The boundary condition for swapping between APS and traditional interleaving PWM control is derived. Based on the simulation studies, a full power range control combining APS and thetraditional interleaving control are proposed. Loss breakdown analysis is also given to exploring the efficiency of the converter. Finally, it is verified by experimental results.

II. Boundary Condition Analysis With Tradition a linter leaving Control:

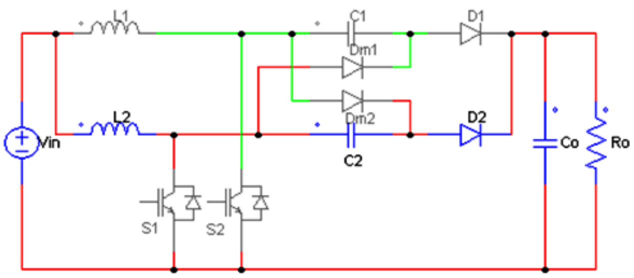
It is assumed that all components in the converter are ideal,both capacitor *C1* and *C2* are large enough, and duty cycle is less than 0.5. The operation of a switching cycle of the converter can be divided into six stages at boundary condition which the voltage stress on switch will be larger than half of the output voltage with traditional interleaving control, as shown in Fig. 2.

1) First Stage (t_0, t_1):

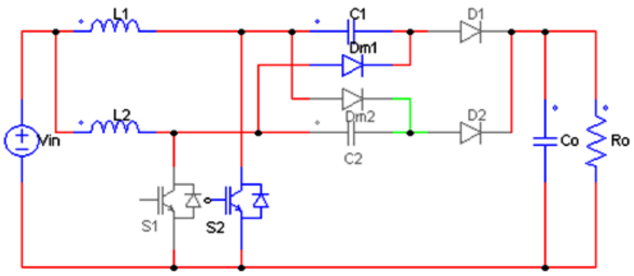
At the moment of t_0, switches$S_1$and $S_2$are off, the energy in the inductor L_2andcapacitor C_2in previous stage are transferred to the outputcapacitor C_0through D_2as shown in Fig. 2(a). The voltagestress on switch $S_1$is the input voltage V_{in}, and the voltagestress on switch S2 is (V_0-V_{C2}), where $V_0$is the output voltage,and $V_{C2}$is the voltage across capacitor (C_2).

2) Second Stage (t_1, t_2):

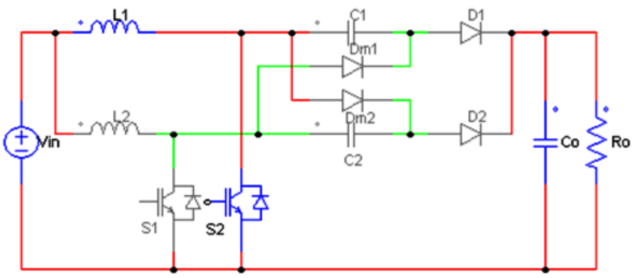
At the moment of t_1, the switch $S_1$is turned on, the inductorL_1starts to store the energy from zero as shown in Fig. 2(b). In the meantime, if (V_{C1}+V_{C2})<V_0, where $V_{C1}$is the capacitor C_1voltage, the diode D_2will be turned off,and diode D_{M2}will be turned on, therefore the energy in the inductor L_2will transferred to the capacitor C_1. If there is enough energy in the inductor L_2, V_{C1}will be charged to the following state: V_{C1}+ V_{C2}≥V_0. Then the D_2will be turned on again, which is shown in Fig. 3. If there is not enough energy to charge $V_{C1}$to (V_0- V_{C2}), then it comes to ThirdStage as shown in Fig. 2(c). If the energy in the inductor $L_2$is discharged to zero and V_{C1}+V_{C2}=V_0at the end of the stage. During the stage, the voltage on switch $S_2$is V_{C1}.



(a) First Stage (t0, t1)



(b) Second Stage (t1, t2)



(c) Third Stage (t2, t3)

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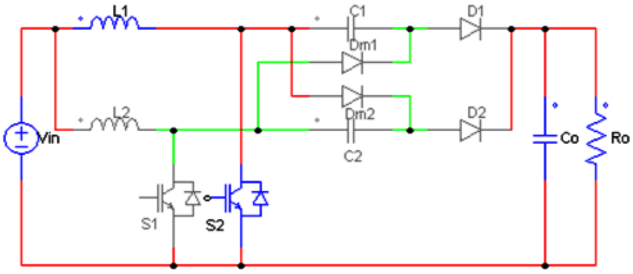
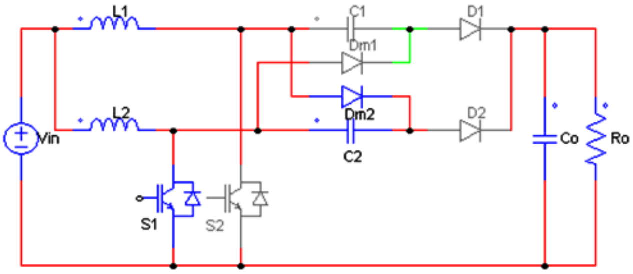
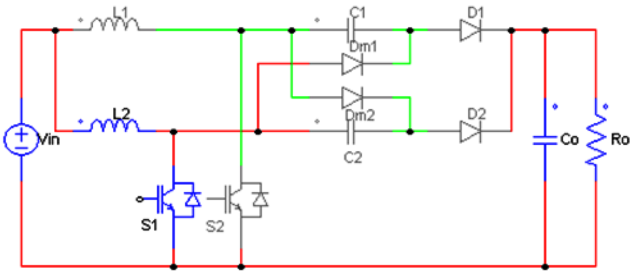


(d) Fourth Stage (t3, t4)



(e) Fifth Stage (t4, t5)



(f) Sixth Stage (t5, t6)

Fig. 2: Stages ofboundary condition.

3) Third Stage (t_2, t_3):

At the moment of t_2, the current in the inductor L_2falls to zero, all the diodes are in off state and the inductor $L_1$is in charging state until the switch $S_1$is turned off at the moment of t_3. The voltage on switch S_2 is V_{in}. At the end of this stage, the current in the inductor L_1 comes to the peak value $I_{L1P}$is

$$I_{L1P} = \frac{V_{in} D_m T_S}{L} \quad (1)$$

Where $V_{in}$is the input voltage, L is the inductance of $L_1$and L_2, $D_m$is the duty cycle, and $T_S$is the switching period.

4) Fourth Stage (t_3, t_4):

At the moment of t_3, switch $S_1$and $S_2$are in off state and the energy in the inductor $L_1$and the capacitor C_1will be transferred to the output capacitor C_0 through the diode D_1, which is similar to First Stage. In this stage, the voltage stress on switch $S_1$is (V_0-V_{C1}), and the voltage stress on switch $S_2$is V_{in}. At the end of this stage, the current in the inductor L_1decreases to be I_{L1M},

$$I_{L1M} = I_{L1P} - \frac{V_0 - V_{C1} - V_{in}}{L}(0.5 - D_M) \quad (2)$$

5) Fifth Stage (t_4, t_5):

At the moment of t_4, the switch $S_2$is turned on, and the inductor L_2starts to store energy. This stage is similar to the Second Stage.The voltage on switch$S_1$is V_{C2}. At the end of thisstage, the current in the inductor L_1decreases to zero from I_{L1M}. And thus

$$I_{L1M} - \frac{V_{C2} - V_{in}}{L}(D_2 - 0.5 + D_m) T_S = 0 \quad (3)$$

Where $D_2$is the duty cycle as shown in Fig. 3.

6) Sixth Stage (t_5, t_6):

At the moment of t_5, the current in the inductor L_1decreased to zero. All the diodes are in off state, and the inductor $L_2$is in charging until the stage comes to the end at the moment t_6. A new switching period will begin with the next First Stage. From the analysis, the voltage sum of capacitor C_1 and C_2will be V_0at boundary condition. If it is less than V_0, the voltage stress on switch $S_1$and S_2will be larger than V_0/2, because the voltage stress on switch $S_1$is (V_0-V_{C1}) during Fourth Stage and the voltage on switch $S_2$is (V_0-V_{C2}) during First Stage. The average value of the output current $i_0$is equal to the DC component of the load current V_0/R, then

$$\frac{V_0}{R} = \frac{1}{T_S}\int_0^{TS} V_0 dt = \frac{1}{T_S}\int_0^{TS} i_1 + i_2 dt$$

$$= \frac{1}{T_S}\int_0^{TS} i_1 dt + \frac{1}{T_S}\int_0^{TS} i_2 dt \quad (4)$$

Considering the same parameters of the circuit in two phases, therefore

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$$\frac{1}{T_S}\int_0^{TS} i_1 dt = \frac{1}{T_S}\int_0^{TS} i_2 dt \qquad (5)$$

By combining the above two, equations,we get as

$$\frac{V_0}{R} = \frac{2}{T_S}\int_0^{TS} i_1 dt = \frac{2}{T_S}\int_{t_3}^{t_4} i_1 dt$$

$$= \frac{2}{T_S}\left[\frac{1}{2}(I_{LIP}+I_{L1M})(0.5-Dm)T_S\right]$$

$$= (I_{LIP}+I_{L1M})(0.5-Dm) \qquad (6)$$

Where *R* is the load.

At boundary condition, the diode $D_2(D_1)$ approaches the conduction state during Second Stage (Fifth Stage), which is shown in Fig. 4.

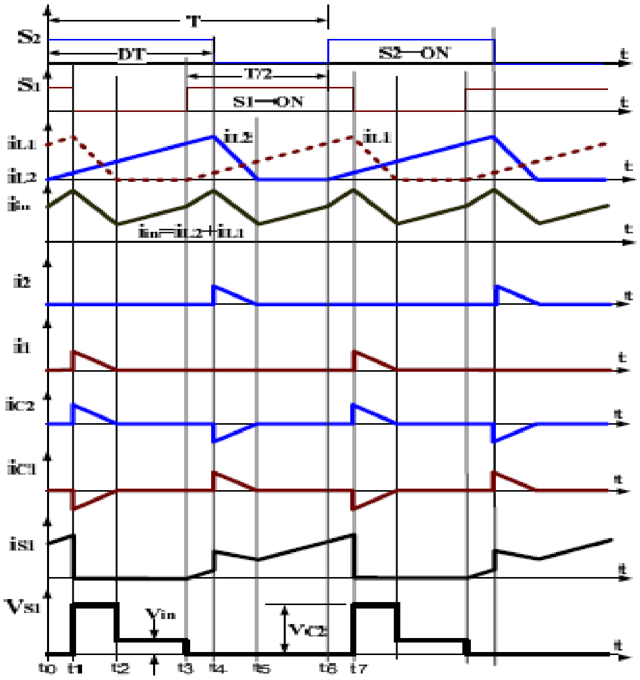

Fig. 3: Main Theoretical Waveforms.

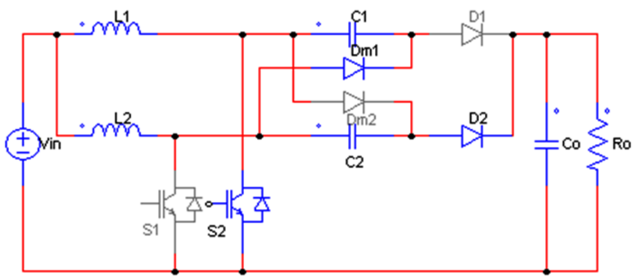

Fig. 4: One stage above boundary condition.

The following equation can be obtained

$$V_{C1}+V_{C2}=V_0 \qquad (7)$$

The capacitors, $C_1$and $C_2$are largeenough, the average voltage of the capacitor will keep equal. Otherwise, the converter will not operate at the boundary condition, therefore

$$V_{C1}= V_{C2}= V_0/2 \qquad (8)$$

By substituting equation (1) and (8) into equation, (2), the current I_{L1M}can be derived as

$$I_{L1M} = \frac{V_{in} - \frac{V_0}{2} + V_0 D_m}{2L} T_s \qquad (9)$$

As shown in Fig. 4, the total discharge of capacitor *C1*between t3 and t4 is

$$Q_{C1} = \int_{t_3}^{t_4} i_{L1}\, dt = \frac{1}{2}(I_{LIP}+I_{L1M})(0.5-D_m)\, T_s \qquad (10)$$

The total charge of capacitor C_2between t_4 and t_5 is

$$Q_{C2} = \int_{t_4}^{t_5} i_{L1} dt = \frac{1}{2} I_{L1M}\,(D_2 - 0.5 + D_m)T_s \qquad (11)$$

According to the analysis, the total discharge of $C_1$is equal to the total charge of capacitor C2 at boundary condition. Therefore, there will be

$$Q_{C1} = Q_{C2} \qquad (12)$$

By combining equation (10), (11) and (12), we get

$$D_2 = (0.5 - D_m)\left(\frac{I_{L1P}}{I_{L1M}} + 2\right) \quad (13)$$

By combining equation (3) and (6) and then substituting equation (1), (9) and (13) into them, the boundary condition can be derived as

$$\left.\begin{aligned} K &= K_{crit} = \frac{n-2}{2n(n-\sqrt{2})^2} \\ D_m &= \frac{n-2}{2n(n-\sqrt{2})} \end{aligned}\right\} \quad (14)$$

Where n is the voltage gain of the converter ($n = V_0/V_{in}$), and$K$ is the parameters of the circuit and $K = 2L/RT_S$.

III. Control Scheme of all Power Range With APS and Traditional Interleaving Control:

According to the principle of APS, APS control is proposed to solve the light load problem with duty cycle less than 0.5 as shown in Fig. 7(a). With the load increasing, the duty cycle will be increased as well. When the duty cycle is increased to 0.5, the APS control will be altered to be a traditional interleaving PWM control with halved switching frequency as shown in Fig. 7(b). According to the previous analysis as shown in Fig. 6, the minimum duty cycle to achieve low voltage stress on switches with the traditional interleaving PWM control is less than 0.5. Therefore, it is possible to combine both APS control and the traditional interleaving PWM controlto control the converter for full power range operation.

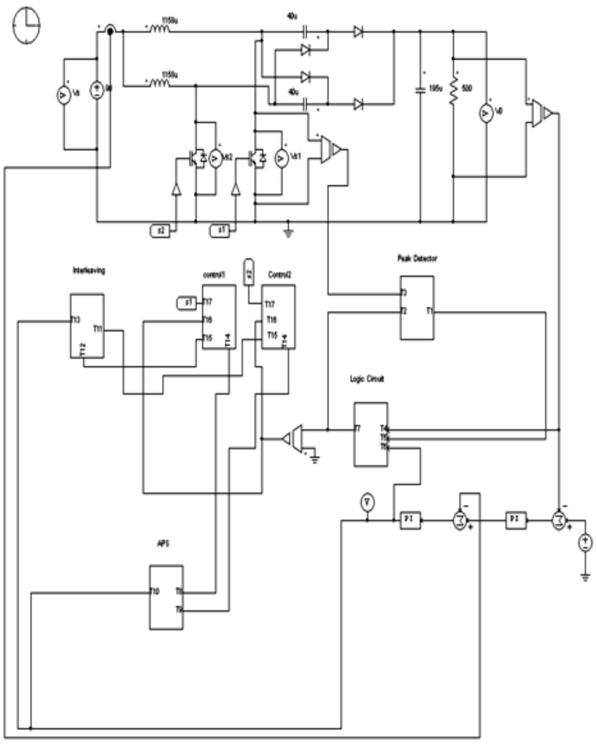

Fig. 5: Block diagram of the converter with the control scheme of all power range.

If APS control mode is used (i.e. *CMP*=1), the optocouplertransistor T1 is turned on, the voltage of capacitor C in the peak detector unit is presented and the peak detector unit is disenabled. If the traditional interleaving control technique is used (i.e. *CMP*=0), the optocoupler transistor T1 will be turned off, and the peak detector unit is enabled and which detects the voltage of switch S1. In order to achieve better dynamic performance operation, dual loop control is adopted as shown in Fig. 8, which inner current loop is to control the input inductor current while the outer voltage loop is to control the output voltage. *Kip* and *Kii* are the PI controller parameters of the inner current loop while *Kip* and *Kvi* are the PI controller parameters of the outer voltage loop.

IV. Simulation Results and Discussions

The circuit parameters are as follows,

V_{in}=100 V

V_0 =700 V

C_1=C_2=40µF

C_0=195µF

L_1=L_2=1158µH

T_s=100µs

H_v=65.536

H_i=698.298

Where *Hv* is the voltage feedback coefficient, and *Hi* is the input current feedback factor. The bandwidth of the inner current loop is 1 kHz with PI parameters as follows: *Kip*=0.061, *Kii*=63.67. The bandwidth of the outer voltage loop is 100 Hz with PI parameters as follows: *Kvp*=4.25*Kvi*=267.036.

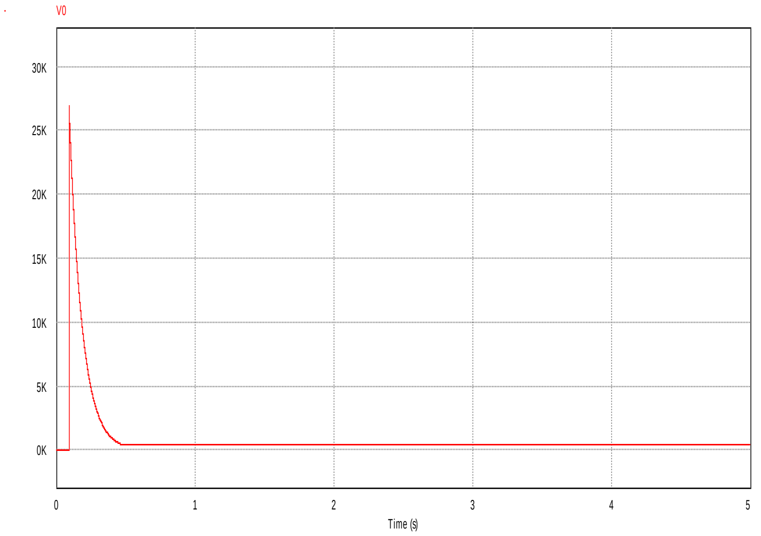

Fig. 6: Output Voltage waveform under Interleaving control and V_{in}=100V.

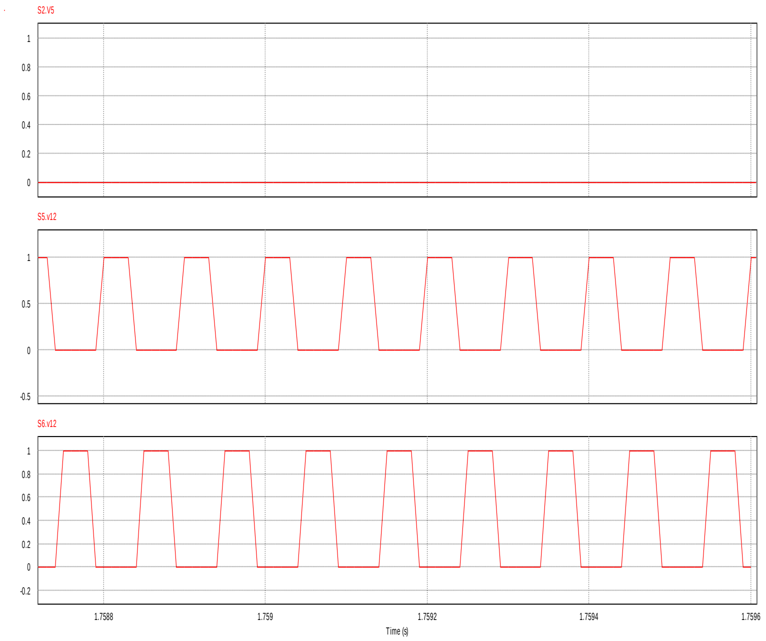

Fig. 7: Output of Logic circuit and PWM Pattern under APS control and V_{in}=100V.

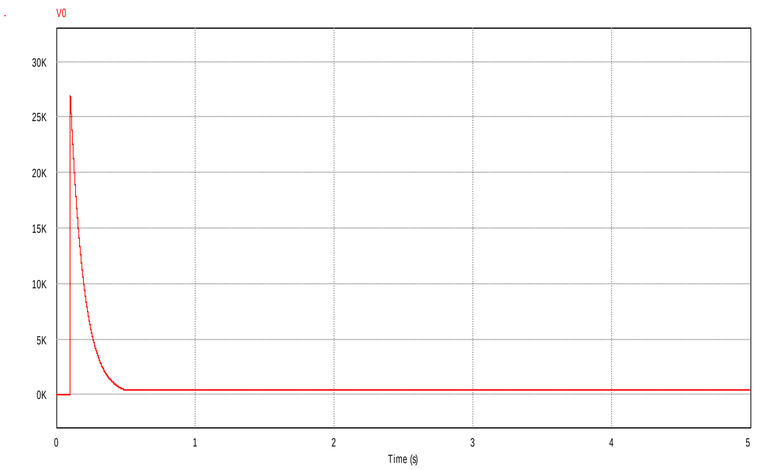

Fig. 8: Output Voltage waveform under Interleaving control and V_{in}=90V.

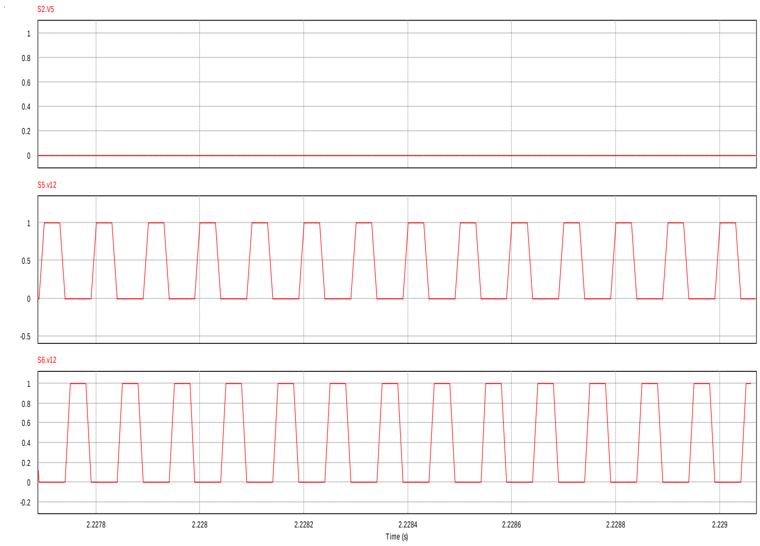

Fig. 9: Output of Logic circuit and PWM Pattern under APS control and V_{in}=90V.

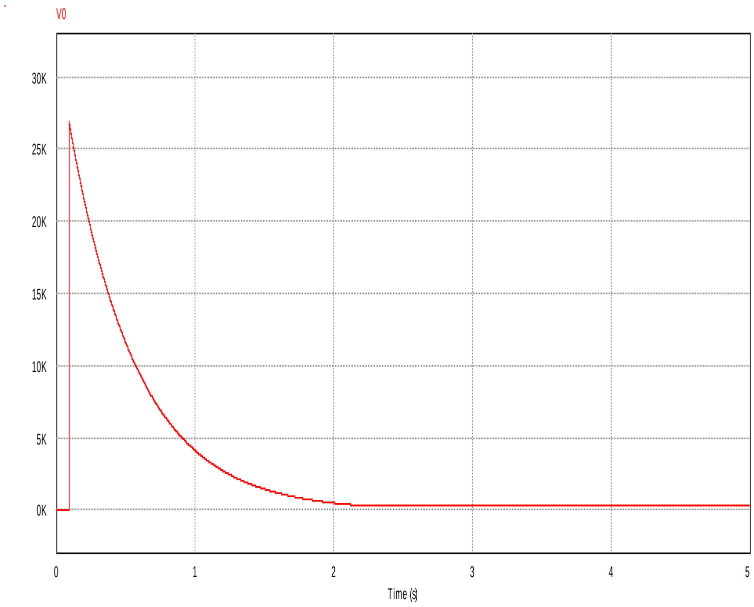

Fig. 10: Output Voltage waveform under APS control and V_{in}=100V.

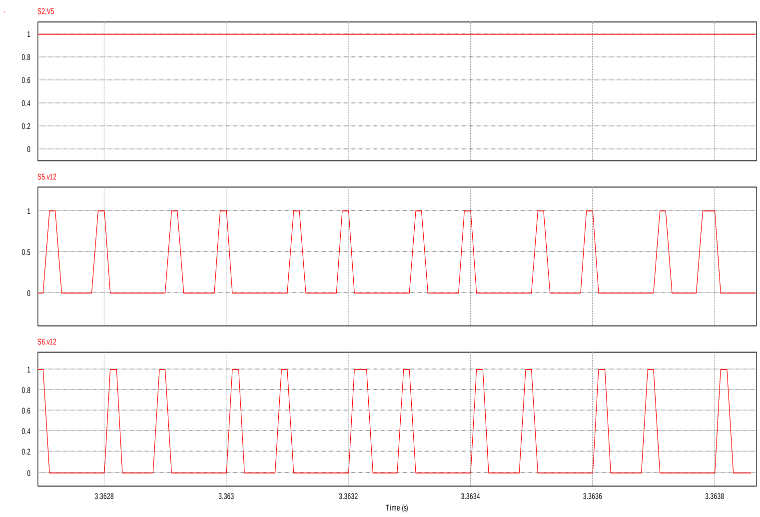

Fig. 11: Output of Logic circuit and PWM Pattern under APS control and V_{in}=100V.

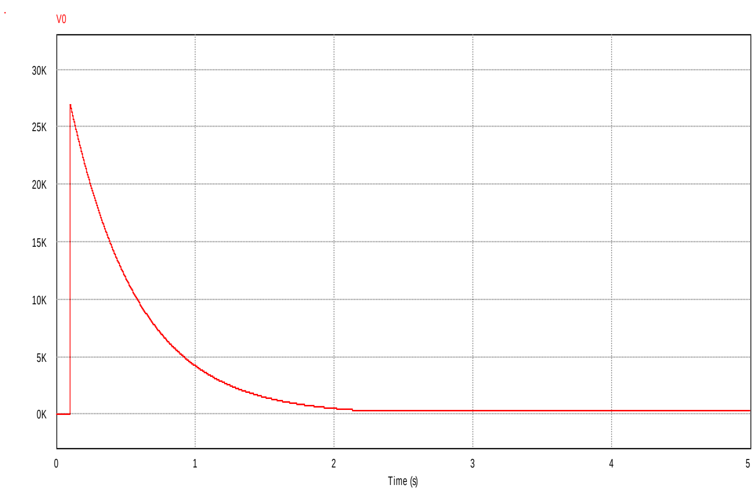

Fig. 12: Output Voltage waveform using APS control andV_{in}=90V.

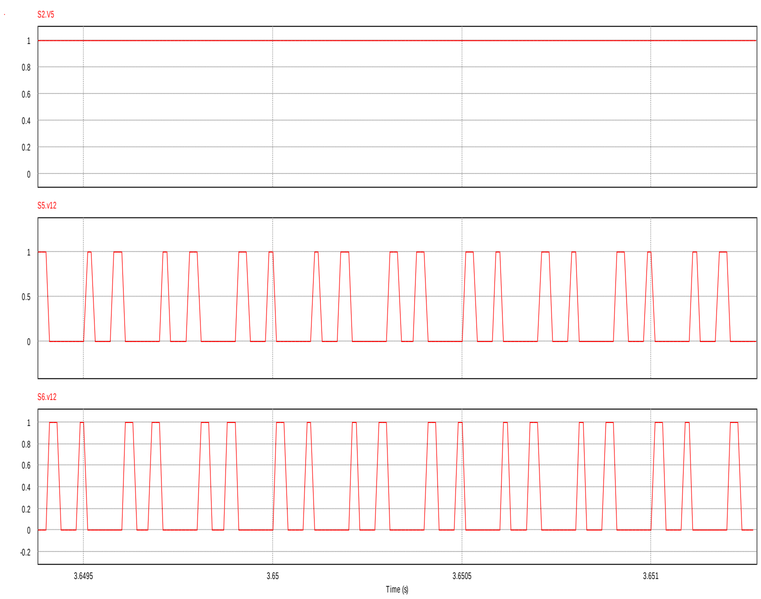

Fig. 13: Output of Logic circuit and PWM Pattern under APS control and V_{in}=90V.

V. Conclusion:

This paper contributes to analysis of multiphase boost converter integrated with a voltage multiplier when it operates in Discontinuous Conduction Mode. From the theoretical analysis, it is shown that the converter cannot achieve expected advantages as in Continuous Conduction Mode (CCM) when light-load is applied with the traditional control method is adopted. A new PWM control method named as Alternating Phase Shift (APS) is proposed to solve the problem. Simulation results show that the proposed control method can solve the light load problem well and could be utilized for full load control with lower voltage stress over the switches.

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